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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/062,714	02/05/2002	Ming-Dou Ker	06720.0070	3110

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EXAMINER
MANDALA, VICTOR A

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/062,714	KER ET AL.	
	Examiner	Art Unit	
	Victor A Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-11 and 16-35* is/are rejected.

7)☒ Claim(s) *7 and 12-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6, 8-11, and 16-35 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,521,952 Ker et al.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

1. Referring to claim 1, an integrated circuit device, comprising: a semiconductor substrate, (Figure 5a #102); an isolation layer, (Figure 5a #128), formed over the semiconductor substrate, (Figure 5a #102); and a layer of silicon material, (Figure 5a #104, 106, 116, 114, 112, 108, and 110), formed over the isolation layer, (Figure 5a #128), including a first p-type portion, (Figure 5a #116), a first n-type portion, (Figure 5a #114), contiguous with the first p-type portion,

(Figure 5a #116), a second p-type portion, (Figure 5a #104), contiguous with the first n-type portion, (Figure 5a #114), a second n-type portion, (Figure 5a #106), contiguous with the second p-type portion, (Figure 5a #104), a third p-type portion, (Figure 5a #108), contiguous with the second n-type portion, (Figure 5a #106), and a third n-type portion, (Figure 5a #110), contiguous with the third p-type portion, (Figure 5a #108), wherein the first, second, and third p-type portions, (Figure 5a #116, 104, and 108), and the first, second, and third n-type portions, (Figure 5a #114, 106, and 110), collectively form a rectifier wherein the first p-type portion, (Figure 5a #116), and the first n-type portion, (Figure 5a #114), form a cathode of the rectifier, and wherein the third n-type portion, (Figure 5a #110), and the third p-type portion, (Figure 5a #108), form an anode of the rectifier.

2. Referring to claim 2, an integrated circuit device, wherein the second p-type portion, (Figure 5a #104), is contiguous with the first p-type portion, (Figure 5a #116).

3. Referring to claim 3, an integrated circuit device, wherein the third n-type portion, (Figure 5a #110), is contiguous with the second n-type portion, (Figure 5a #106).

4. Referring to claim 4, an integrated circuit device, wherein the second p-type portion, (Figure 5a #104), includes the first n-type portion, (Figure 5a #114), and the first p-type portion, (Figure 5a #116), each of which being spaced apart from the isolation layer, (Figure 5a #128).

5. Referring to claim 5, an integrated circuit device, wherein the second p-type portion, (Figure 5a #104), additionally includes a fourth n-type portion, (Figure 5a #112), spaced apart from the first n-type portion, (Figure 5a #114), the first n-type portion, (Figure 5a #114), and the fourth n-type portion, (Figure 5a #114), defining a source region and a drain region of an NMOS transistor.

6. Referring to claim 6, an integrated circuit device, wherein the second n-type portion, (Figure 5a #106), includes the third n-type portion, (Figure 5a #110), and the third p-type portion, (Figure 5a #108), each of which being spaced apart from the isolation layer, (Figure 5a #128).

7. Referring to claim 8, an integrated circuit device, wherein the first n-type portion, (Figure 5a #114), and the first p-type portion, (Figure 5a #116), are contiguous with the isolation layer, (Figure 5a #128).

8. Referring to claim 9, an integrated circuit device, wherein the second p-type portion, (Figure 5a #104), includes a fourth n-type portion, (Figure 5a #112), formed spaced apart from the first n-type portion, (Figure 5a #114), and wherein the first n-type portion, (Figure 5a #114), and the fourth n-type portion, (Figure 5a #112), define a source region and a drain region of an NMOS transistor.

9. Referring to claim 10, an integrated circuit device, wherein the NMOS transistor comprises a gate, (Figure 5a #120), for receiving a voltage to turn on the NMOS transistor.

10. Referring to claim 11, an integrated circuit device, wherein the third n-type portion, (Figure 5a #110), and the third p-type portion, (Figure 5a #108), are contiguous with the isolation layer, (Figure 5a #128).

11. Referring to claim 16, an integrated circuit device, further comprising at least one isolation portion, (Figure 5a #128), formed contiguous with the rectifier.

12. Referring to claim 17, an integrated circuit device, comprising: a semiconductor substrate, (Figure 5a #102); an isolation layer, (Figure 5a #128), formed over the semiconductor substrate, (Figure 5a #102), an n-type MOS transistor, (Figure 5a #123), having a gate, (Figure

5a #120), a drain region and a source region, (Figure 5a #114 & 112), formed over the isolation layer, (Figure 5a #128); and a p-type MOS transistor, (Figure 5a #124), having a gate, (Figure 5a #124), a drain region and a source region, (Figure 5a #112 & 108), formed over the isolation layer, (Figure 5a #128), and contiguous with the n-type MOS transistor, (Figure 5a #123), wherein the n-type MOS transistor, (Figure 5a #123), and the p-type MOS transistor, (Figure 5a #124), form a rectifier to provide electrostatic discharge protection.

13. Referring to claim 18, an integrated circuit device, further comprising an electrostatic discharge circuit for providing the bias voltage to trigger the rectifier, the electrostatic discharge circuit comprising a first inverter, (Figure 11b examiner's label #1500), including a first PMOS transistor, (Figure 11b examiner's label #1501), having a gate, (Figure 11b examiner's label #1502), a source region, (Figure 11b examiner's label #1509), and a drain region, (Figure 11b examiner's label #1508), and a first NMOS transistor, (Figure 11b examiner's label #1503), having a gate, (Figure 11b examiner's label #1504), a source region, (Figure 11b examiner's label #1510), and a drain region, (Figure 11b examiner's label #1511), wherein the gate, (Figure 11b examiner's label #1502), of the first PMOS transistor, (Figure 11b examiner's label #1501), is coupled, (Figure 11b examiner's label #1507), to the gate, (Figure 11b examiner's label #1504), of the first NMOS transistor, (Figure 11b examiner's label #1503), and the gate, (Figure 11b examiner's label #1502), of the p-type MOS transistor, (Figure 11b examiner's label #1501), is coupled, (Figure 11b examiner's label #1505), to the drain region, (Figure 11b examiner's label #1508), of the first PMOS transistor, (Figure 11b examiner's label #1501), and the drain region, (Figure 11b examiner's label #1511), of the first NMOS transistor, (Figure 11b examiner's label #1503).

14. Referring to claim 19, an integrated circuit device, wherein the gate of the p-type MOS transistor, (Figure 11b examiner's label #1502), is coupled to receive the bias voltage to trigger the rectifier to provide electrostatic discharge protection, (Col. 3 Lines 41-44).

15. Referring to claim 20, an integrated circuit device, wherein the electrostatic discharge circuit further comprises a second inverter, (Figure 11b #772), including a second PMOS transistor having a gate, a source region and a drain region, and a second NMOS transistor having a gate, a source region and a drain region, wherein the gate of the second PMOS transistor is coupled to the gate of the second NMOS transistor, and the gate of the n-type MOS transistor is coupled to the drain region of the second PMOS transistor and the drain region of the second NMOS transistor, (Same as in rejected claim 18 but for inverter # 772).

16. Referring to claim 21, an integrated circuit device, wherein the source region, (Figure 11b examiner's label #1510), of the first NMOS transistor, (Figure 11b examiner's label #1502), is coupled to ground, (Figure 11b VSS).

17. Referring to claim 22, an integrated circuit device, wherein the source region, (Figure 11b examiner's label #1520), of the second NMOS transistor, (Figure 11b examiner's label #1523), is coupled to ground, (Figure 11b VSS).

18. Referring to claim 23, an integrated circuit device, wherein the source region, (Figure 11b examiner's label #1508), of the first PMOS transistor, (Figure 11b examiner's label #1501), is coupled to a pad to receive an electrostatic current, (Figure 11b VDD).

19. Referring to claim 24, an integrated circuit device, wherein the source region, (Figure 11b examiner's label #1521), of the second PMOS transistor, (Figure 11b examiner's label #1522), is coupled to a pad to receive an electrostatic current, (Figure 11b VDD).

20. Referring to claim 25, an integrated circuit device, further comprising a first n-type region, wherein one of the source region and the drain region of the p-type MOS transistor, (Figure 5a #108), and the first n-type region, (Figure 5a #110), form an anode of the rectifier.

21. Referring to claim 26, an integrated circuit device, further comprising an electrostatic discharge circuit for providing the bias voltage to trigger the rectifier, the electrostatic discharge circuit comprising a first inverter, (Figure 11b examiner's label #1500), including a first PMOS transistor, (Figure 11b examiner's label #1501), having a gate, (Figure 11b examiner's label #1502), a source region, (Figure 11b examiner's label #1509), and a drain region, (Figure 11b examiner's label #1508), and a first NMOS transistor, (Figure 11b examiner's label #1503), having a gate, (Figure 11b examiner's label #1504), a source region, (Figure 11b examiner's label #1510), and a drain region, (Figure 11b examiner's label #1511), wherein the gate, (Figure 11b examiner's label #1502), of the first PMOS transistor, (Figure 11b examiner's label #1501), is coupled, (Figure 11b examiner's label #1507), to the gate, (Figure 11b examiner's label #1504), of the first NMOS transistor, (Figure 11b examiner's label #1503), and the gate, (Figure 11b examiner's label #1504), of the n-type MOS transistor, (Figure 11b examiner's label #1503), is coupled to the drain region, (Figure 11b examiner's label #1508), of the first PMOS transistor, (Figure 11b examiner's label #1501), and the drain region, (Figure 11b examiner's label #1511), of the first NMOS transistor, (Figure 11b examiner's label #1503).

22. Referring to claim 27, an integrated circuit device, wherein the anode of the rectifier, (Figure 11b examiner's label #1508 & Figure 5a #108 & 110), coupled to the gate, (Figure 11b examiner's label #1502), of the p-type MOS transistor, (Figure 11b examiner's label #1501).

23. Referring to claim 28, an integrated circuit device, wherein the gate, (Figure 11b examiner's label #1504), of the first NMOS transistor, (Figure 11b examiner's label #1503), and the gate, (Figure 11b examiner's label #1502), of the first PMOS transistor, (Figure 11b examiner's label #1501), are coupled in parallel to a resistor, (Figure 11b examiner's label #1530), and a capacitor, (Figure 11b examiner's label #1531).

24. Referring to claim 29, an integrated circuit device, wherein the anode, (Figure 11b examiner's label #1508), of the rectifier is coupled to a pad, (Figure 11b Vdd), to receive an electrostatic current.

25. Referring to claim 30, an integrated circuit device, further comprising an electrostatic discharge circuit for providing a bias voltage to trigger, (Col. 3 Lines 61-63), the rectifier to provide electrostatic discharge protection, wherein the gate, (Figure 11b examiner's label #1504), of the n-type MOS transistor, (Figure 11b examiner's label #1503), is coupled to receive the bias voltage.

26. Referring to claim 31, an integrated circuit device, further comprising a first p-type region, wherein one of the source region and the drain region, (Figure 5a #114), of the n-type MOS transistor, (Figure 5a #123), and the first p-type region, (Figure 5a #116), form a cathode of the rectifier.

27. Referring to claim 32, an integrated circuit device, wherein the cathode is coupled to at least one diode, (Figure 11b #766), to prevent the rectifier from being triggered in a non-ESD operation.

28. Referring to claim 33, a method for protecting a silicon-on-insulator semiconductor circuit from electrostatic discharge, comprising: providing an n-type MOS transistor, (Figure 11b

examiner's label #1503), having a source region, (Figure 11b examiner's label #1509), and a drain region, (Figure 11b examiner's label #1508), in the silicon-on-Insulator, (Figure 5a #128), circuit; providing a p-type MOS transistor, (Figure 11b examiner's label #1501), having a source region, (Figure 11b examiner's label #1510), and a drain region, (Figure 11b examiner's label #1511), the p-type MOS transistor, (Figure 11b examiner's label #1501 and Figure 5a #124), being contiguous with the n-type MOS transistor, (Figure 11b examiner's label #1503 and Figure 5a #123); providing a p-type region, (Figure 5a #116), contiguous with one of the source region and the drain region, (Figure 5a #114), of the n-type MOS transistor, (Figure 11b examiner's label #1503 and Figure 5a #123), to form a cathode; and providing an n-type region contiguous, (Figure 5a #110), with one of the source region and the drain region, (Figure 5a #108), of the p-type MOS transistor, (Figure 11b examiner's label #1501 and Figure 5a #124), to form an anode, wherein the n-type region, (Figure 5a #110), the p-type region, (Figure 5a #116), the p-type MOS transistor, (Figure 11b examiner's label #1501 and Figure 5a #124), and the n-type MOS transistor, (Figure 11b examiner's label #1503 and Figure 5a #123), form a rectifier.

29. Referring to claim 34, a method, further comprising a step of biasing the p-type MOS transistor, (Figure 11b examiner's label #1501), to trigger the rectifier, (Col. 3 Lines 41-44).

30. Referring to claim 35, a method, further comprising a step of biasing the n-type MOS transistor, (Figure 11b examiner's label #1503), to trigger the rectifier, (Col. 3 Lines 61-63).

Allowable Subject Matter

Claims 7and 12-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent Application Publication No. 2003/0007301 and U.S. Patent No. 6,242,763.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (703) 308-6560. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

VAMJ
June 1, 2003